frequency in accordance with the current generated by the charge pump, and wherein the PLL circuit has a first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use, the method comprising the steps of:

detecting a high impedance state of the charge pump; and

switching the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.

4. (Amended) A circuit for controlling the mode of a PLL circuit, wherein the PLL circuit includes a phase comparator for comparing the phase of a reference frequency-divided signal and the phase of a comparison frequency-divided signal with each other and generating a comparison output signal, a charge pump connected to the phase comparator, for generating a current depending on the comparison output signal from the phase comparator, and a voltage-controlled oscillator connected to the charge pump, for generating an output signal having a predetermined frequency in accordance with the current generated by the charge pump, and wherein the PLL circuit has a first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use, the circuit comprising:

a state detecting circuit for detecting a high impedance state of the charge pump, and generating a mode switching signal to switch the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.

19. (Amended) A semiconductor device comprising:

a PLL circuit; and

a mode control circuit connected to the PLL circuit, for controlling switching of the mode of the PLL circuit; wherein the PLL circuit includes:

a phase comparator for comparing the phase of a reference frequency-divided signal and the phase of a comparison frequency-divided signal with each other and generating a comparison output signal,

a charge pump connected to the phase comparator, for generating a current depending on the result of the comparison by the phase comparator, and

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a voltage-controlled oscillator connected to the charge pump, for generating an output signal having a predetermined frequency in accordance with the current generated by the charge pump, wherein the PLL circuit has a first mode for locking an output signal thereof up to a desired frequency at a high speed and a second mode in normal use; and

wherein the mode control circuit detects a high impedance state of the charge pump, and generates a mode switching signal to switch the mode of the PLL circuit from the first mode to the second mode or from the second mode to the first mode when the high impedance state is detected.

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